## REMARKS

Claims 1 through 50 are currently pending in the application.

Claims 17, 18, 25, 42, 43 and 50 have been withdrawn from consideration as being directed to a non-elected invention.

Claims 1 through 16, 19 through 24, 26 through 41, and 44 through 49 currently stand rejected.

This amendment is in response to the Office Action of March 16, 2004.

**Information Disclosure Statement(s)**

Applicant notes the filing of two Information Disclosure Statements herein on August 29, 2001 and August 22, 2002 and notes that copies of the PTO-1449s were not returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449s be made of record herein.

**35 U.S.C. § 102(b) Rejections**

Anticipation Rejection Based on Yamada et al. (U.S. Patent 5,864,178)

Claims 1-3, 5-8, 10-12, 14-16, 20, 21, 23, 24, 26-28, 30-33, 35-37, 39-41 and 45-49 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yamada et al. (U.S. Patent 5,864,178).

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicant further asserts that the identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to the Yamada et al. reference, described is a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing filler. In FIGS. 56A through 56D a semiconductor chip 201 is mounted on a wiring circuit board 202 using bumps 203 with the semiconductor chip 201 having a layer of a first resin 204 constituting a laminate of

encapsulation resin, a second layer of resin 205 on the wiring circuit board 202 constituting a laminate of encapsulation resin, a third encapsulation resin 206 constituting a laminate of encapsulation resin applied to a portion of the second layer of resin 205, a polymer film 207 formed on the semiconductor chip 201, and a polymer film 208 formed on the wiring circuit board 202. Nowhere does Yamada et al. describe the semiconductor chip 201 having at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wettable by a polymeric material. At best, Yamade et al. describe that solely the first layer of encapsulation resin 204, second layer of encapsulation resin 205, and third encapsulation resin 206 may include a silane coupling agent therein mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. Nowhere in the Yamada et al. reference is there any description whatsoever directed to any of the encapsulation resins 204, 205, and 206 acting as a wetting agent under any circumstances.

Applicant asserts that the Yamada et al. reference does not and cannot anticipate the presently claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 under 35 U.S.C. § 102 because the Yamada et al. reference does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. For instance, Applicant asserts that the Yamada et al. reference does not identically describe the elements of the presently claimed inventions set forth in independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for "the semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wettable by a polymeric material", "a wetting agent layer provided on said active surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer and wettable by a polymeric material", "a wetting agent located on a portion of said active surface of said semiconductor device", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device, the underfill material substantially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer

provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wettable by a polymeric material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of about a monolayer and wettable by a polymeric material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor die", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate", and "a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate".

In contrast to the claimed inventions, Applicant asserts that nowhere, either expressly or inherently, does the Yamada et al. reference describe a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Yamada et al. reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin. Therefore, the Yamada et al. reference cannot and does not anticipate under 35 U.S.C. § 102 the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

**35 U.S.C. § 103(a) Rejections**

Obviousness Rejection Based on Estes et al. (U.S. Patent 6,410,415) in view of Wong et al. (U.S. Patent 6,180,696)

Claims 4, 9, 13, 19, 22, 29, 34, 38, 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Estes et al. (U.S. Patent 6,410,415) in view of Wong et al. (U.S. Patent 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turing to the cited prior art, the Estes Patent teaches or suggests a semiconductor assembly having an IC chip 1 including an active surface having at least one bond pad 6 and at least one bump 2 attached thereto. The bump 2 connects one bond pad on the active surface of the IC chip 1 to the substrate bond pads 4 on a substrate 3. An electrically insulating adhesive 5 is provided between the substrate 3 and the IC chip 1.

The Wong reference teaches or suggests an epoxy base polymeric composition/formulation with a curing peak temperature ranging from 180°C to 240°C, suitable rheologic characteristics and excellent fluxing activity, which meets the requirements of the no-flow underfilling process for low melting point solder bumps such as with eutetic tin/lead alloy. The epoxy base polymeric composition/formulation includes a silane coupling agent to improve the adhesion between a semiconductor die and the under fill material. The Wong reference does not teach or suggest the use of a silane coupling agent except as part of the epoxy base polymeric composition/formulation.

Applicant asserts that no combination of the Estes et al. reference and the Wong reference establishes a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 because, at the very least, any combination of the cited prior art fails to teach or suggest all of the claim limitations of the inventions set forth in such independent claims.

For instance, Applicant asserts that any combination of the Estes et al. reference and the Wong reference fails to teach the claim limitations of the inventions set forth in independent claims , 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for "the semiconductor device having

an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wettable by a polymeric material", "a wetting agent layer provided on said active surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer and wettable by a polymeric material", "a wetting agent located on a portion of said active surface of said semiconductor device", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device, the underfill material substantially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wettable by a polymeric material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of about a monolayer and wettable by a polymeric material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor die", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate", and "a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate".

In contrast to the claimed inventions, Applicant asserts that nowhere does any combination of the Estes et al. reference and the Wong reference teach or suggest a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Wong reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin. Therefore, the Estes et al. reference and the Wong reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45,

and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

Yet further, the Estes et al. reference fails to teach or suggest a wetting agent layer of about a monolayer thick that is wettable by a polymeric material to teach or suggest the presently claimed inventions under 35 U.S.C. § 103.

In contrast to the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48, the Estes et al. reference generally discloses an electrically insulating adhesive 5 located between an IC chip 1 and a circuit board (substrate 3). The Estes reference does not disclose a monolayer thick wetting agent layer having the specific wetting properties as recited in presently amended claims 1 and 26. Neither does the Wong reference teach or suggest a wetting agent layer of about a monolayer thick that is wettable by a polymeric material. Additionally, no combination of the Estes et al. reference and the Wong reference teaches or suggests a wetting agent layer of about a monolayer thick that is wettable by a polymeric material. Therefore, presently amended independent claims 1, 26, and 31 and claims depending therefrom are not taught or suggested by any combination of the Estes et al. reference and the Wong reference.

Similarly, presently amended independent claims 6 and 31 recite the limitation "a wetting agent layer provided on said active surface of said semiconductor, said wetting agent layer having a thickness of about a monolayer and wettable by a polymeric material." As stated above, the Estes reference or the Wong reference fails to teach or suggest a monolayer thick wetting agent layer having the specific wetting properties recited in the presently amended independent claims 6 and 31. Therefore, presently amended independent claims 6 and 31 and claims depending therefrom are not taught or suggested by any combination of the Estes et al. reference and the Wong reference.

Presently amended independent claims 10 recites the limitations of "a wetting agent located on a portion of said active surface of said semiconductor device; and
an underfill material substantially filling a volume located between said substrate and said wetting agent." Similarly, presently amended independent claim 14 recites the limitations of "a wetting agent layer provided on at least a portion of said active surface of said semiconductor

device, the underfill material substantially filling a volume between the wetting agent layer and said upper surface of said substrate."

The any combination of Estes et al. reference and the Wong reference fails to teach or suggest a wetting agent or wetting agent layer located on a portion of the active surface of IC chip 1 and an underfill material filling a volume between the wetting agent or wetting agent layer and the substrate 3. The Estes reference merely discloses electrically insulating adhesive 5 disposed between the IC chip 1 and the substrate 3. The Estes reference does not teach or suggest disclose an intervening wetting agent or wetting agent layer between electrically insulating adhesive 5 and IC chip 1. Neither does the Wong reference teach or suggest an intervening wetting agent layer. Therefore, presently amended independent claims 10 and 14 and claims depending therefrom are not taught or suggested by any combination of the Estes et al. reference and the Wong reference.

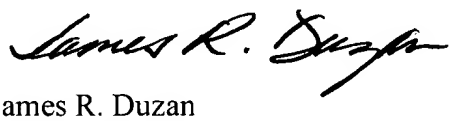
Presently amended independent claim 35 recites the limitations "a wetting agent located on a portion of said active surface of said semiconductor die; and an underfill material located between said substrate and said semiconductor die." Presently amended independent claim 39 recites the limitations of an underfill material provided between said substrate and said semiconductor die; and a wetting agent layer provided on at least a portion of said active surface of said semiconductor die."

The Estes et al. reference fails to teach or suggest disclose a wetting agent or a wetting agent layer located on a portion of the active surface of its IC chip 1 and an underfill material disposed between its IC chip 1 and substrate 3. In contrast, the Estes et al reference teaches or suggests electrically insulating adhesive 5 filling the space between the IC chip 1 and substrate 3. Neither does the Wong reference teach or suggest a wetting agent or wetting agent layer. Therefore, presently amended independent claims 35 and 39 and claims depending therefrom are not taught or suggested by any combination of the Estes et al. reference and the Wong reference. taught or suggested by any combination of the Estes et al. reference and the Wong reference.

## CONCLUSION

Applicant submits that claims 1 through 50 are clearly allowable over the cited prior art. Applicant requests the allowance of claims 1 through 50 and the case passed for issue.

Respectfully submitted,



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